

WHAT IS CLAIMED IS:

1 1. A memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances, comprising the steps:

4 obtaining a first parametric dataset for a
5 first plurality of memory compilers, each of said memory
6 compilers for compiling a respective memory instance
7 having a select number of physical rows and a select
8 number of physical columns, wherein each memory instance
9 is organized using a first MUX factor and each data point
10 in said first parametric dataset corresponds to said
11 respective memory instance, said data point comprising a
12 value with respect to a particular parameter;

13 obtaining a second parametric dataset by
14 characterizing said particular parameter for a second
15 plurality of memory compilers, each of said second
16 plurality of memory compilers for compiling a respective
17 memory instance organized with a second MUX factor,
18 wherein said second plurality of memory compilers are
19 sampled from said first plurality of memory compilers
20 such that each memory instance compiled by said second
21 plurality of memory compilers corresponds to a respective
22 congruent memory instance of said first parametric
23 dataset having identical numbers of physical rows and
24 physical columns;

25 determining scale factors for a select number
26 of parametric data points associated with respective

27 congruent memory instances of said first and second
28 parametric datasets;

29 obtaining an interpolated scale factor based on
30 said scale factors; and

31 deriving a value of said particular parameter
32 for an additional memory instance of second parametric
33 dataset by applying said interpolated scale factor to a
34 data point associated with a memory instance of said
35 first parametric dataset, wherein said memory instance is
36 congruent with respect to said additional memory instance
37 of said second parametric dataset.

1 2. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein said
4 particular parameter comprises a memory timing parameter.

1 3. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 2, wherein said
4 memory timing parameter comprises memory access time.

1 4. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 2, wherein said
4 memory timing parameter comprises memory cycle time.

1 5. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein said
4 first MUX factor is selected from the group consisting of
5 a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a
6 MUX-32 factor.

1 6. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein said
4 second MUX factor is selected from the group consisting
5 of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a
6 MUX-32 factor.

1 7. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a read-only memory (ROM) circuit.

1 8. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a static random access memory (SRAM)
6 circuit.

1 9. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a dynamic random access memory (DRAM)
6 circuit.

1 10. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein each
4 memory instance of said first and second parametric
5 datasets comprises an electrically programmable ROM
6 (EPROM) circuit.

1 11. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a flash memory circuit.

1 12. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein each
4 memory instance of said first and second parametric
5 datasets comprises an embedded memory circuit.

1 13. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a stand-alone memory circuit.

1 14. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein said
4 interpolated scale factor is obtained by interpolating
5 four scale factors, each corresponding to a ratio of
6 values of said particular parameter for a pair of
7 congruent memory instances.

1 15. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 1, wherein said
4 step of obtaining said first parametric dataset and said
5 step of obtaining said second parametric dataset are
6 effectuated by characterization of said particular
7 parameter via simulation.

1 16. A memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances, comprising the steps:

4 obtaining a first parametric dataset for a
5 first plurality of memory compilers representative of a
6 first memory technology, each of said memory compilers
7 for compiling a respective memory instance having a
8 select number of physical rows and a select number of
9 physical columns and organized using a select MUX factor,
10 wherein each data point in said first parametric dataset
11 corresponds to said respective memory instance, said data
12 point comprising a value with respect to a particular
13 parameter;

14 obtaining a second parametric dataset by
15 characterizing said particular parameter for a second
16 plurality of memory compilers that are representative of
17 a second memory technology, each of said second plurality
18 of memory compilers for compiling a respective memory
19 instance organized with said select MUX factor, wherein
20 said second plurality of memory compilers are sampled
21 from said first plurality of memory compilers such that
22 each memory instance compiled by said second plurality of
23 memory compilers corresponds to a respective congruent
24 memory instance of said first parametric dataset having
25 identical numbers of physical rows and physical columns;

26 determining scale factors for a select number
27 of parametric data points associated with respective

28 congruent memory instances of said first and second
29 parametric datasets;

30 obtaining an interpolated scale factor based on
31 said scale factors; and

32 deriving a value of said particular parameter
33 for an additional memory instance of second parametric
34 dataset by applying said interpolated scale factor to a
35 data point associated with a memory instance of said
36 first parametric dataset, wherein said memory instance is
37 congruent with respect to said additional memory instance
38 of said second parametric dataset.

1 17. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein said
4 particular parameter comprises a memory timing parameter.

1 18. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 17, wherein said
4 memory timing parameter comprises memory access time.

1 19. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 17, wherein said
4 memory timing parameter comprises memory cycle time.

1 20. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein said
4 select MUX factor is selected from the group consisting
5 of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a
6 MUX-32 factor.

1 21. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a read-only memory (ROM) circuit.

1 22. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a static random access memory (SRAM)
6 circuit.

1 23. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a dynamic random access memory (DRAM)
6 circuit.

1 24. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein each
4 memory instance of said first and second parametric
5 datasets comprises an electrically programmable ROM
6 (EPROM) circuit.

1 25. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a flash memory circuit.

1 26. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein each
4 memory instance of said first and second parametric
5 datasets comprises an embedded memory circuit.

1 27. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein each
4 memory instance of said first and second parametric
5 datasets comprises a stand-alone memory circuit.

1 28. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein said
4 interpolated scale factor is obtained by interpolating
5 four scale factors, each corresponding to a ratio of
6 values of said particular parameter for a pair of
7 congruent memory instances.

1 29. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein said
4 step of obtaining said first parametric dataset and said
5 step of obtaining said second parametric dataset are
6 effectuated by characterization of said particular
7 parameter via simulation.

1 30. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein said
4 first memory technology is selected from the group
5 consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ
6 technology and 0.2 μ technology.

1 31. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein said
4 second memory technology is selected from the group
5 consisting of 1.0 μ technology, 0.8 μ technology, 0.6 μ
6 technology and 0.2 μ technology.

1 32. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein said
4 first and second memory technologies comprise design-
5 rule-specific technologies.

1 33. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein said
4 first and second memory technologies comprise foundry-
5 specific technologies.

1 34. The memory compiler characterization method for
2 determining parametric data associated with compilable
3 memory instances as set forth in claim 16, wherein said
4 first and second memory technologies comprise process-
5 flow-specific technologies.

1 35. A memory compiler characterization system,
2 comprising:

3 means for characterizing a first plurality of
4 memory compilers with respect to a particular parameter,
5 said first plurality of memory compilers for compiling
6 memory instances of a first type;

7 means for characterizing a second plurality of
8 memory compilers with respect to said particular
9 parameter, said second plurality of memory compilers for
10 compiling memory instances of a second type, wherein said
11 memory instances of second type comprise memory instances
12 sparsely sampled from said memory instances of first type
13 such that each memory instance of second type corresponds
14 to a respective congruent memory instance of first type
15 having identical numbers of physical rows and physical
16 columns;

17 means for determining scale factors between
18 values of said particular parameter respectively
19 associated with a sample of congruent memory instances of
20 said first and second types;

21 an interpolator to obtain an interpolated scale
22 factor based on said scale factors; and

23 means for obtaining a value of said particular
24 parameter for an additional memory instance of second
25 type by utilizing said interpolated scale factor in
26 conjunction with a parametric value of a congruent memory
27 instance of first type which corresponds to said
28 additional memory instance.

1 36. The memory compiler characterization system as
2 set forth in claim 35, wherein said memory instances of
3 first type comprise memory instances with a first MUX
4 factor and said memory instances of second type comprise
5 memory instances with a second MUX factor.

1 37. The memory compiler characterization system as
2 set forth in claim 36, wherein said first MUX factor is
3 selected from the group consisting of a MUX-4 factor, a
4 MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

1 38. The memory compiler characterization system as
2 set forth in claim 36, wherein said second MUX factor is
3 selected from the group consisting of a MUX-4 factor, a
4 MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

1 39. The memory compiler characterization system as
2 set forth in claim 35, wherein said memory instances of
3 first type comprise memory instances associated with a
4 first memory technology and said memory instances of
5 second type comprise memory instances associated with a
6 second memory technology.

1 40. The memory compiler characterization system as
2 set forth in claim 39, wherein said first memory
3 technology is selected from the group consisting of 1.0 μ
4 technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ
5 technology.

1 41. The memory compiler characterization system as
2 set forth in claim 39, wherein said second memory
3 technology is selected from the group consisting of 1.0 μ
4 technology, 0.8 μ technology, 0.6 μ technology and 0.2 μ
5 technology.

1 42. The memory compiler characterization system as
2 set forth in claim 39, wherein said first and second
3 memory technologies comprise design-rule-specific
4 technologies.

1 43. The memory compiler characterization system as
2 set forth in claim 39, wherein said first and second
3 memory technologies comprise process-flow-specific
4 technologies.

1 44. The memory compiler characterization system as
2 set forth in claim 39, wherein said first and second
3 memory technologies comprise foundry-specific
4 technologies.

1 45. The memory compiler characterization system as
2 set forth in claim 35, wherein said memory instances
3 comprise one of a DRAM circuit, an SRAM circuit, a ROM
4 circuit, an EPROM circuit and a flash memory circuit.

1 46. A computer-accessible medium operable in
2 connection with a processor environment, said computer-
3 accessible medium carrying a sequence of instructions
4 which, when executed in said processor environment, cause
5 the following steps to be performed:

6 characterizing a first plurality of memory
7 compilers with respect to a particular parameter, said
8 first plurality of memory compilers for compiling memory
9 instances of a first type;

10 characterizing a second plurality of memory
11 compilers with respect to said particular parameter, said
12 second plurality of memory compilers for compiling memory
13 instances of a second type, wherein said memory instances
14 of second type comprise memory instances sparsely sampled
15 from said memory instances of first type such that each
16 memory instance of second type corresponds to a
17 respective congruent memory instance of first type having
18 identical numbers of physical rows and physical columns;

19 determining scale factors between values of
20 said particular parameter respectively associated with a
21 sample of congruent memory instances of said first and
22 second types;

23 obtaining an interpolated scale factor based on
24 said scale factors; and

25 deriving a value of said particular parameter
26 for an additional memory instance of second type by
27 applying said interpolated scale factor in conjunction
28 with a parametric value of a congruent memory instance of

29 first type which corresponds to said additional memory
30 instance.

1 47. The computer-accessible medium as set forth in
2 claim 46, wherein said memory instances of first type
3 comprise memory instances with a first MUX factor and
4 said memory instances of second type comprise memory
5 instances with a second MUX factor.

1 48. The computer-accessible medium as set forth in
2 claim 46, wherein said memory instances of first type
3 comprise memory instances associated with a first memory
4 technology and said memory instances of second type
5 comprise memory instances associated with a second memory
6 technology.

1 49. The computer-accessible medium as set forth in
2 claim 46, wherein said memory instances comprise one of
3 a DRAM circuit, an SRAM circuit, a ROM circuit, an EPROM
4 circuit and a flash memory circuit.